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# Parallel SPP Model Design of Data Acquisition Experiment Device

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***Abstract:*** **Using parallel SPP mode switch to input and output experiment device can simulate the collected data, and according to the principle of data acquisition program, the acquisition of data for storage, query processing, output, etc. The simulation data can be used as environmental temperature, humidity, pressure and individual traits such as a variety of experimental data of a certain parameter values or attribute value. Independent research and development of experimental apparatus are curriculum design. For example expansion form C language demonstration to Visual C++ language, after around simulation data collected by deepening the reform of computer learning.**

***Keywords:*** Computer Practice; Visual C++; Data Acquisition; Standard Parallel Port (SPP)

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## 1. Introduction

Communication interface between the data acquisition system and a computer can have a variety of ways, such as serial, parallel, ISA bus. Choose which kind of communication interface is closely related to the way the data acquisition system. Laptop, notebook computer, with its features of light weight, convenient carrying and good generality, can satisfy the requirement of data collection of anytime and anywhere. But due to the lack of data acquisition in laptop and notebook need built-in ISA expansion slot, the use of laptop and notebook computer serial port or standard parallel port SPP.

The current domestic and foreign application main goal is that return the practice of teaching reform, adapt to the need of the industry status and development [1] in the information age, pay attention to open to the students' participation, guidance, teaching process and cooperation incentive to cultivate the students' learning autonomy, optional sex and compound. University in our country is the developing trend of the research university, To cultivate students can attach importance to practice, to practice, fall in love with practical attitude, make full interest in using of the demonstration example, actively looking for opportunities, further encourage students want to do more, put the idea into practice, make innovation spirit rise to innovation [2]. Master the operation of characteristic of computational thinking, guide to put forward new problems.

## 2. Technical Background

Parallel interface was first used as a standard interface, thanks to Centronics manufacture of printers using a simple parallel bus interface in the market a lot of use. More parallel port expansion datasheet can still claim to be compatible with Centronics. With the demand for two-way data transmission, parallel port also began to use two-way parallel port transmission protocol, and produced a series of enhanced and extended specifications, including SPP (Standard Parallel Port).

### *2.1. Standard Parallel Port Design Base*

SPP is the standard mode of the parallel port, also known as compatibility mode or Centronics standard mode. Data is from the computer one-way transmission. Using the data line for data input, Centronics mode data transmission is a positive way, the parallel interface standard a total of 36 Pin signals. In the system connection, the receiver is a 36-pin D-type socket, the host end is a 25-pin D-type socket.

The parallel port provides eight data lines for parallel byte data transfer. The master sends the first pin of the 25-pin data cable to the external device. The transmission signal (STROBE) informs the external device that the data is ready, which is called the strobe signal. After the external device receives the data, it must return a signal (ACK) to the computer as the response, which is called the response signal.

### *2.2. Standard Parallel Port Structure Design*

SPP mode is a master-slave structure; data transmission is a non-reciprocal relationship between the two sides. Data transfer can only be started by the computer, but peripherals can't start the data transfer as well. If the peripherals to carry out data transmission, can only apply to the computer to interrupt, and then start the data transfer by the computer.

If the external device is not busy, then the host write control register, the output trigger signal nSTROBE, the data to write to the data register, then read the status register to check the BUSY signal, if the external



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device is not busy, the host write control register, output trigger signal nSTROBE, the data write Into an external device. Thus, in order to output a byte, you need four I/O instructions and some additional instructions, handshaking signals by the software, the maximum transmission rate is 150 kbit /s.

Standard configuration of existing computer parallel ports have three port registers of eight bit, including the data registers, the status registers and the control registers, the computer can read and write by the register to access the data of the parallel port. In many cases directly using the existing computer complete data input and output port is not impossible to achieve, must pass a certain conversion device to achieve. The utility model to solve the technical problem is to provide a data acquisition experiment device, the use of the device can realize parallel SPP model switch input and output [3].

### *2.3. The technical scheme of the utility model*

The device including rectangular shell, shell on the top with the order for D7 ~ D0 just eight location identification. Below the location identification is equipped with upper and lowers two rows and the location identification should be relatively light, ranked as the output light, discharge to the input light. Under two rows of lights for the eight data input KD series switches, KD series switch settings are respectively with the D7~D0 location identification should be relatively, each KD series switch is equipped with two switch input state 1 or 0. On the sidewalls of the shell has a connection port and the device's start switch.

As shown in Figure 1, the device including rectangular shell logo1 is on the top with the order for D7~D0 eight positioning logo 2. Below the target logos 2 is equipped with upper and lower two rows and the target logo 2 corresponding indicator light, for the output light is logo3, on the bottom of input light is logo 4. Under two rows of lights for the eight data input KD series switch is logo 5, KD series switch settings are respectively correspond to the D7 ~ D0 positioning logo 2, each logo 5 KD series switch is equipped with two switch input state 1 or 0. When a state of KD series switch to 1, the above input indicator; when the series KD, the state of the switch for 0, above the input light is not bright. On the sidewalls of the shell 1 is equipped with the terminals logo 6 and start switch logo 7 of the device. When Kn (n = 0,..., 7) input 1, Dn location input indicator; Otherwise Dn position light is put out. OUT LED lights for the output data, works the same as the input data indicator.

### *2.4. The principle of the utility model*

The experimental system in the standard parallel port of computer SPP mode, using the data port D0~D7, a total of 8 bits for data output from the computer to the experiment device; Using control port C0~C3, a total of four control and state port (S3~S64 state a splicing into eight bits (C0~C3 for high four, S3 ~S6 for low 4 bit) implement the data from experiment device to the computer's input.

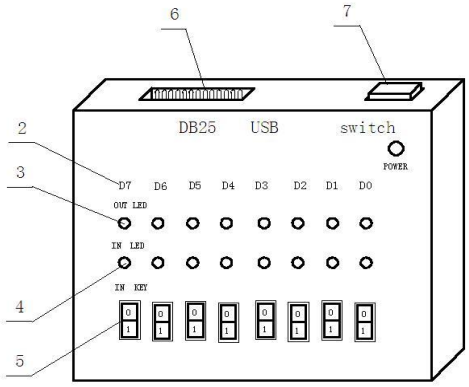


**Figure 1. SPP model switch input and output.**

As shown in figure 2, OUT0~OUT7 for experiment data output pin; IN0~IN7 the data of experimental device input pin. On-off signal data from experiment device IN0~ N7 pin standard by computer parallel port connector pins as P15, P13, P12, P10, P1, P14, P16 and P17 into computer standard parallel port status register S3~S6 and control registers C0~C3. By programming control and status registers can be read and spliced into 1 byte of eight bit in the data. Then, the data will be joining together after processing the data through the program written data registers D0~D7, this data by the computer standard parallel port connector pins P2~P9 was introduced into experimental apparatus OUT0~OUT7 pins, so as to realize the data from experiment device of computer parallel port to standard output.

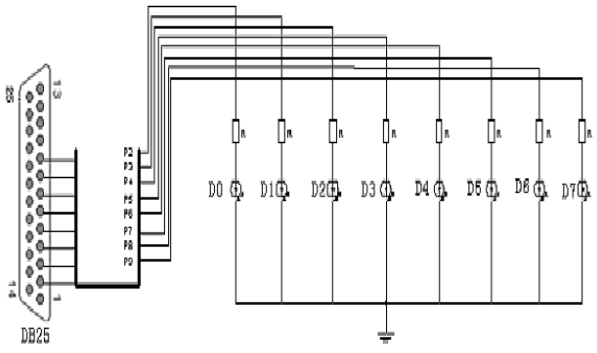


**Figure 2. SPP model's principle.**

## 3. Using Installation Instructions and Method

Now, Standard configuration of existing computer parallel port has three port registers of eight bits. Respectively: data registers, state registers and control registers. The computer can read and write by the register to access the data of the parallel port. In many cases directly using the existing computer complete data input and output port is not impossible to achieve,



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but can pass a certain conversion device to achieve.

### *3.1. C ++ program interface design platform*

First, start the computer, enter the Windows environment, if you use the object-oriented programming languages such as Visual C++, Visual VB ect. If you use the TC process oriented programming language, should better enter the Dos environment. Then, connect the DB25 end of the experiment device with the computer standard parallel port connection; Connect the USB port and the computer's USB port; Open experiment device the Power Switch, the Switch again to check the Power indicator light (Power), if the indicator, indicates the experimental device can work normally. At this time, you can start using the experiment device.

This module is done by the historyload () function. It is a friend of the class List function, directly on the List of private members to operate. User input to open the file name after historyload () function to ios :: in | ios :: nocreate way to open the file (that is, step (3)). Next, the first file >> n, read the file stored in the total number of data; then, in turn read the data and encapsulate them respectively SHUJU class object built, and then use the pointer to transfer these objects linked with List Link . Each load a set of data historyload () will load the data screen output.

### *3.2. Standard parallel port design*

For example, the use of K0 ~ K7, KD switch to collect data such as 23 degrees (corresponding the binary number as 00010111), press the corresponding KD switch place K4, K1, K2, K0 is 1, place K7, K6, K5, K3 is 0; Make the light D4, D2 and D0 input bright, implement the data input; Operate the program to write data standard parallel port of computer data as 23, make the output of OUT LED correspond indicator D4, D2 and D0 , so as to realize the data output. Parallel port connector with a total of 25 pins, the interface appearance is shown in Figure 3.

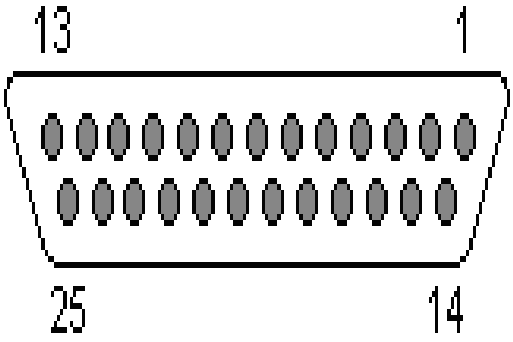


**Figure 3. Standard parallel port 25 pin type D socket.**

### *3.3. Register work timing fast reading and writing*

The workings of a computer parallel port can be set in the BIOS SETUP to SPP model configuration. The corresponding I/O port was to use the same base address SPP, and an increase in the back of the five ports. First three port (b+ /00h~02h0) compatible with SPP, but can two-way transmission, respectively is SPP/EPP data, state and control. Fourth port (b+ /3h0) is the address of the EPP port, the fifth port (b+ /04h0) is the EPP data, after three port (b+ /5h~7h0) undefined. If work in four or five ports way, its typical transfer rate of 500kB/s~2MB/s, and two-way work, close to the PC of the ISA bus data transfer rate, this is one of the major features of EPP protocol. EPP use 4 or 5 ports.

**Table 1 Data port pin definition**

| Register tag | Connector pins | Signal | Signal source | Inverter connector |
|---|---|---|---|---|
| D0 | P2 | Data0 | PC | No |
| D1 | P3 | Data1 | PC | No |
| D2 | P4 | Data2 | PC | No |
| D3 | P5 | Data3 | PC | No |
| D4 | P6 | Data4 | PC | No |
| D5 | P7 | Data5 | PC | No |
| D6 | P8 | Data6 | PC | No |
| D7 | P9 | Data7 | PC | No |

Provides four kinds of data transfer cycle, i.e., data write cycle, data read cycle, address write cycle, read cycle.4, 5 port works, can be carried out fast and two-way data transmission, data read and address cycle, for example, the difference is different, the data read (b+4) produce DATASTB signals, and address read (b+3) produce ADDRSTB signals. Other exactly the same, as for the data read back D0~D7 as address or as data, completely decided by the designer. Data read, for example, the working process of the to maintain a high level remains unchanged, the WRITE signal if the WAIT is low, data gating signal DATASTB become low; WAIT WAIT from low to high (at this point should be put WAIT high), the falling edge of the WAIT release the data line, end of the read cycle.

### *3.4. Data register port design*

Data register is also called the data port. Acquiesce in address as 378 H, its definition as shown in Table 1.

Through the signal /BUSY, /ACK, /STROBE reasonable judgment, can W intercept data effectively. /ACK signals for the trigger or introduce/ACK signal of master control chip, external interrupt pin is rising along the arrival trigger external interruption, the system began to collect valid data. Although the definition of the signal with the pattern varies, but the response signal/ACK, represented the meaning of the same Status register: status register is also called the state port, the default address as 379 H, its definition as shown in Table 2.



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**Table 2 State port pin definition**

| Register tag | Connector pins | Signal | Signal source | Inverter connector |
|---|---|---|---|---|
| S0 | | Time-Out | | |
| S1 | | unused | | |
| S2 | | unused | | |
| S3 | P15 | nError(nFault) | peripherals | No |
| S4 | P13 | Select | peripherals | No |
| S5 | P12 | PaperEnd | peripherals | No |
| S6 | P10 | nAck | peripherals | No |
| S7 | P11 | Busy | peripherals | Yes |

By the work timing of SPP mode when/ACK signal rise along the ACK signal, trigger mode is configured to rising along the trigger. Article 8 if cable directly connected to the I/O port, due to the constant change of the data, collected data in the interrupt service function will appear error. And latch the data staging, to maintain a certain level, the output latch status will not change along with the change of input, only in the state of the latch signal input is saved to the output, it was not until the next latch signal arrival to change. Control register: control register is also called the console port, the default address as 37AH, its definition as shown in Table 3.

**Table 3 Control port pin definition**

| Register tag | Connector pins | Signal | Signal source | Inverter connector |
|---|---|---|---|---|
| C0 | P1 | nStrobe | PC | Yes |
| C1 | P14 | nAutoLF | PC | Yes |
| C2 | P16 | nInit | PC | No |
| C3 | P17 | nSelectIn | PC | Yes |
| C4 | | IRQ | | |
| C5 | | unused | | |
| C6 | | unused | | |
| C7 | | unused | | |

### *3.5. Application of practice teaching*

SPP mode is used to simulate and collect the data, and the data acquisition program is programmed according to its principle. The data are stored, inquired and output processed by the parallel port SPP mode digital input/output experimental device. The simulated data can be used as an index value or attribute value for various experimental data such as temperature, humidity, pressure, or individual traits of the seed. You can focus on the different meaning of analog data collection design problems and achieve the relevant design content.

This experiment device for the student can be extended to real related to the design of the topic, formulate feasible development course design plan, review the related textbooks and reference books, such as:

I. Determine the topic, set up the design team, make the requirement analysis (0.5 days);

II. Internet access to information, analyze problems, formulate solutions (1 day);

III.Program and debug (3 days);

IV.Submit design content and improvement (1 day).

Automation major, after the early stage of learning C++ language was very interested in the experiment, the group on the basis of the original TurboC, using Visual C++ 6.0 to write the performance measurement, output, sorting, and query information, and through the file record measurement information and summary. Divided into a responsible: measurement module (innew () function); Data storage module; Join together of each module; Data input module; Data statistics module; Output module. Analyzed by the List class innew () function is complete, the function calls the Winio library function: GetPortVal (0 x379, & getval, 1); CTRLG x37a SetPortVal (0, 1); A friend function using the class List, private members of the List.

## 4. Conclusion

Ease of use, the firmware is easy to maintain, etc. With a high level of integration, Windows interface development system, the C++ style code, automatically generated program scheduling mechanism etc, greatly reduces the development. The soft to develop flexible configuration function, product wind risk is smaller.

Based on increased course in all kinds of professional curriculum design process, in order to can reach the practical exploration or project for the outline of the topic, so that the students in the design process has a clear train of thought, through the practice data feedback to prove the study effect is good, eventually to foster and train students' ability of autonomous learning. Due to previous experimental verification, more students have no development design thought and ability. In shorter design time, improve the practice teaching of practical methods, to strengthen and perfect the practice teaching link of the teaching effect.

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